NS – 345

I Semester B.Sc. Examination, November/December 2016
(CBCS) (2014-15 and Onwards) (F+R)
ELECTRONICS – I
Basic Electronics

Time : 3 Hours Max. Marks : 70

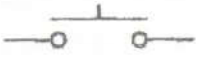
Instruction : *Answer **all** questions from Part – **A**, **any five** from Part – **B** and **any four** questions from Part – **C**.*

Note : *Answer **all** questions of Part – **A** in **any one** page, the **same** question answered multiple times will **not** be considered for evaluation.*

PART – A

1. Answer **all** the sub-divisions : **(15×1=15)**

i) The following circuit symbol represents



a) An SPDT switch b) a DPDT switch
c) a Push to ON switch d) a Push to OFF switch

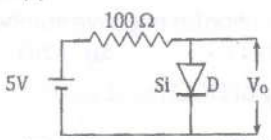
ii) Miniature Circuit Breaker (MCB) acts as a
a) toggle switch b) transformer c) relay d) fuse

iii) Norton's equivalent circuit consists of a
a) constant current source with a conductance in parallel
b) constant voltage source in parallel with high resistance
c) a current source with an voltage source
d) constant current source in series with infinite resistance

iv) According to KVL, the algebraic sum of all IR drops and EMFs in any closed loop of a network is always
a) zero b) positive c) negative d) equal to unity

v) The Superposition theorem is essentially based on
a) duality b) linearity c) reciprocity d) non-linearity

vi) Approximate value of output voltage in the circuit shown is



a) 20 V b) 10 V c) 0.7 V d) 1.7 V

P.T.O.

vii) Theoretical value of ripple factor for a Half Wave Rectifier is
a) 0.482 b) 0.812 c) 1.11 d) 1.21

viii) Second approximation of a silicon diode is represented by
a) only a dc source of 0.7 V
b) dc source of 0.7 V in series with an ideal diode
c) only a series resistance
d) a dc source of 0.7 V parallel with a resistance

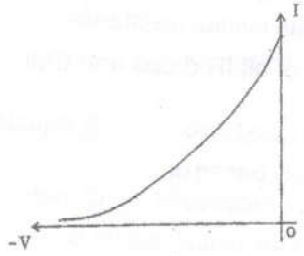
ix) Voltage regulator is a circuit which
a) converts the a.c. voltage to d.c. voltage
b) smoothens the variations in d.c. output voltage
c) maintains a constant d.c. output voltage
d) converts d.c. to a.c.

x) In a Bipolar Junction Transistor,
a) Emitter is moderate in size and heavily doped
b) Emitter is larger in size and heavily doped
c) Emitter is smaller in size and heavily doped
d) Emitter is smaller in size and lightly doped

xi) The leakage current I_{CBO} flows in
a) the emitter, base and collector leads
b) the emitter and base leads
c) the emitter and collector leads
d) the base and collector leads

xii) A Field-Effect Transistor (FET) operates using
a) majority carriers only b) minority carriers only
c) positively charged ions only d) negatively charged ions only

xiii) The device which exhibits the following transfer characteristics is
a) Diode b) BJT c) Zener diode d) JFET



xiv) 4 bit representation in Sign magnitude convention for negative number, +7 is
a) 0111 b) 1101 c) 1111 d) 1010

xv) The next consecutive number in the array of BCD numbers 0111, 1000, 1001 is
a) 1111 0001 b) 1011 0001 c) 1110 d) 0001 0000

PART – B

Answer **any five** questions : **(5×7=35)**

2. a) Explain the method of conversion of a current source into a voltage source.
   b) Draw the circuit diagram, write the expression for the growth and decay of current in a series RL circuit and show them graphically. Define 'time constant'. **(2+5)**

3. Draw a series RLC circuit and write the condition for resonance. Show the resonance curve graphically and write the expressions for
   i) Resonance frequency
   ii) Bandwidth
   iii) Quality factor

4. a) State superposition theorem.
   b) State Thevenin's theorem. With suitable circuit diagrams, explain the steps to Thevenise a resistive network. **(2+5)**

5. a) With a circuit diagram and necessary waveforms, explain the operation of Shunt capacitor filter.
   b) Draw the circuit diagram of series transistor voltage regulator. **(2+5)**

6. a) Draw the block diagram of a Regulated power supply.
   b) With a circuit diagram, explain the working of center-tap full wave rectifier. Sketch the input and output waveforms. **(2+5)**

7. a) Explain the need for biasing in transistors.
   b) Obtain the expressions for the operating point of a transistor voltage divider bias circuit. **(2+5)**

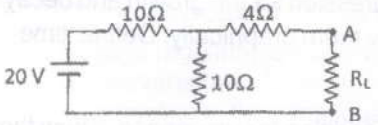
8. With necessary diagrams, explain the working of a JFET and define the parameters r_d, g_m and μ.

9. a) Explain with an example, the conversion of a decimal number into its Hexadecimal equivalent.
   b) Write the Excess 3 code equivalents for all the Decimal digits. **(4+3)**

PART – C

Answer **any four** questions : **(4×5=20)**

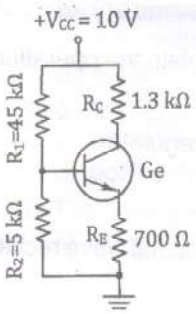
10. Determine value of R_L for Maximum power transfer in the following circuit, Also calculate the Maximum power delivered to the load.



11. An ac voltage of 150 V and 50 Hz frequency is applied to a series RL circuit having L = 2 H and R = 20 Ω. Calculate the impedance, current and phase angle.

12. Calculate (i) efficiency and (ii) PIV of a Half wave rectifier circuit with an input voltage of 200 volt rms and load R_L of 75 Ω. Given $r_d = 5\,\Omega$. The turns ratio of the transformer is 10 : 1.

13. Draw the D.C. load line and mark the operating point for the biasing circuit shown. Given : $\beta = 250$



14. Perform the Subtraction of following binary numbers using 2's complement method.
    a) $11100_{(2)} - 10011_{(2)}$ b) $1001_{(2)} - 1100_{(2)}$
    Express the results in decimal system.

15. a) Convert the following binary numbers into Hexadecimal
        i) $110101001_{(2)}$ ii) $1100111_{(2)}$
    b) Convert the following decimal numbers into binary
        i) $67.3_{(10)}$ ii) $78.60_{(10)}$ **(2+3)**